SUBSTRATE DURING GATE STACK ETC

Inventor: Pan et al.

Serial No.: 09/073,494

Docket No.: 2269-2915.1US



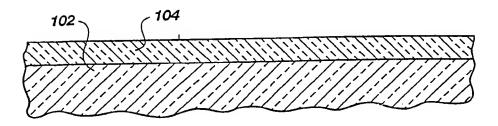
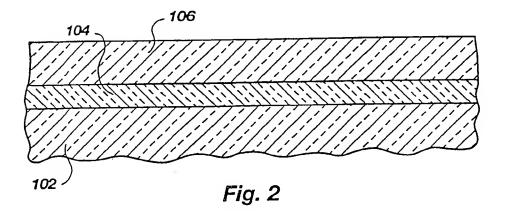


Fig. 1

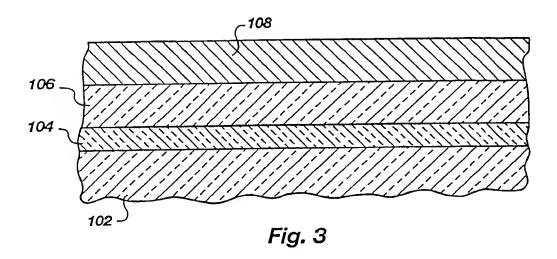


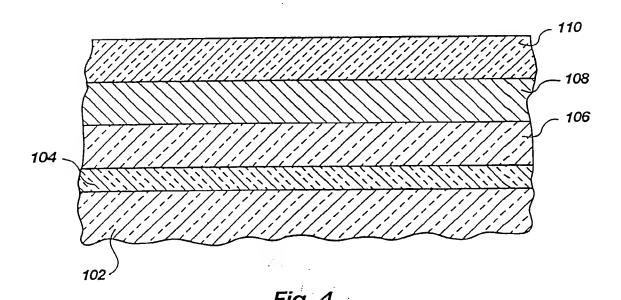


Inventor: Pan et al. Serial No.: 09/073,494 Docket No.: 2269-2915.1US









TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

SUBSTRATE DURING GATE STAC Inventor: Pan et al.

Serial No.: 09/073,494 Docket No.: 2269-2915.1US



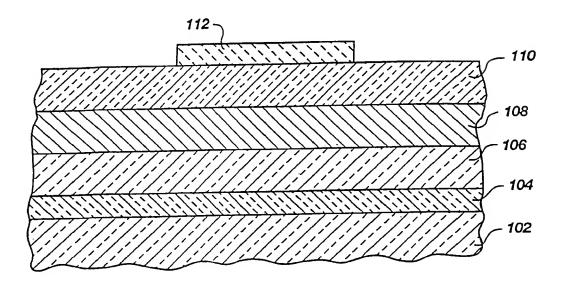


Fig. 5

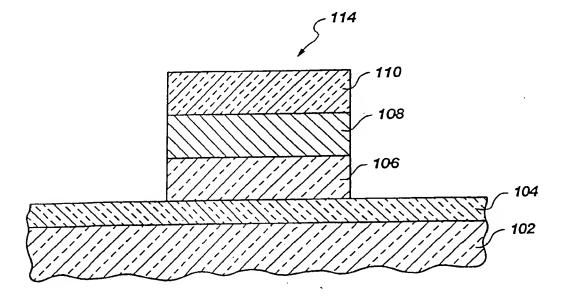


Fig. 6

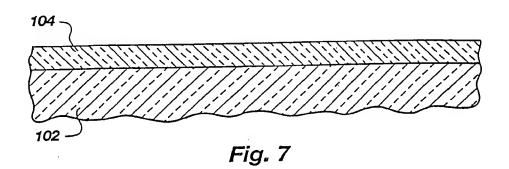
SUBSTRATE DURING GATE STACK ETCH Inventor: Pan et al.

Serial No.: 09/073,494

Docket No.: 2269-2915.1US







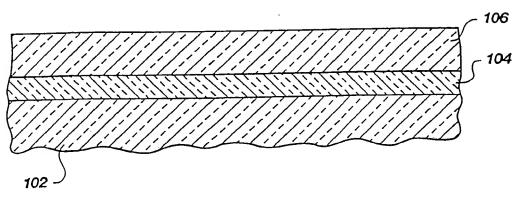
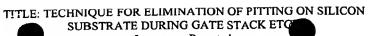


Fig. 8





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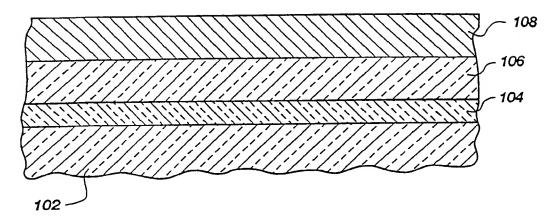


Fig. 9

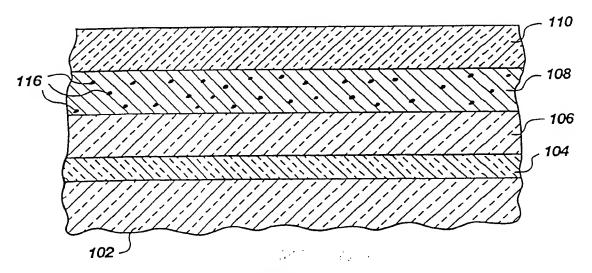
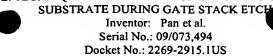


Fig. 10

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON



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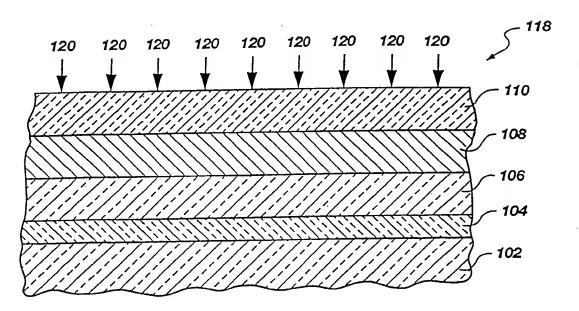


Fig. 11

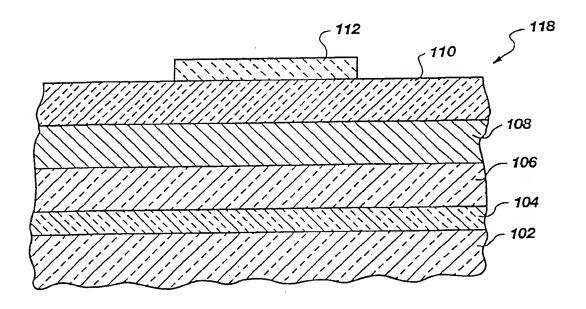


Fig. 12

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETC

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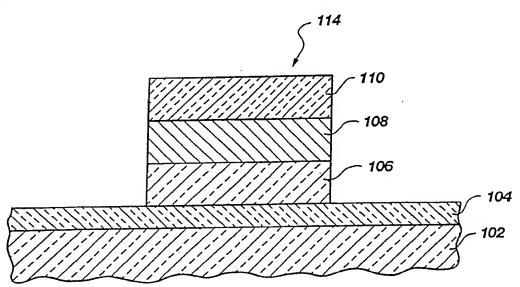


Fig. 13

THE TECHNIQUE FOR ELIMINATION OF PITTING ON STAILON SUBSTRATE DURING GATE STACK ETCH

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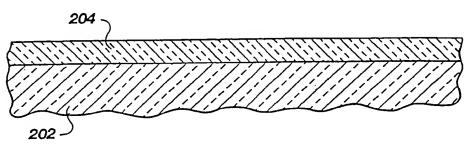
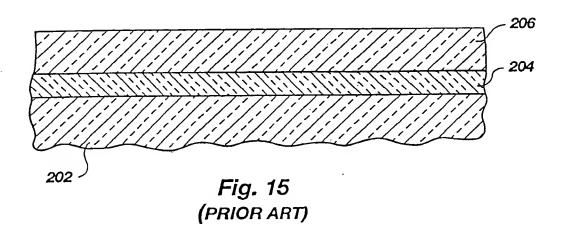


Fig. 14 (PRIOR ART)



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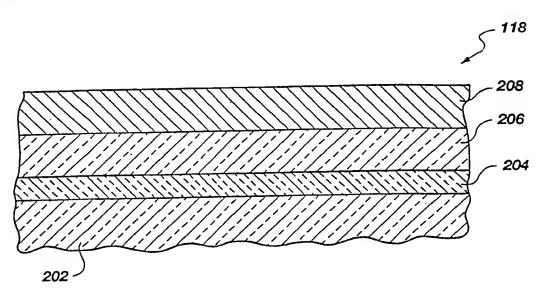


Fig. 16
(PRIOR ART)

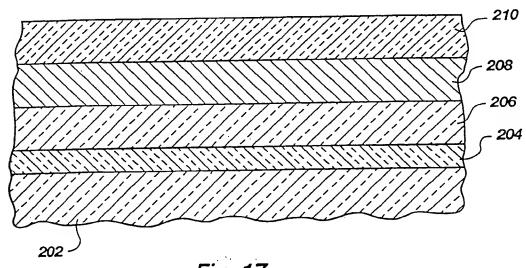


Fig. 17 (PRIOR ART)

SUBSTRATE DURING GATE STACK ETC



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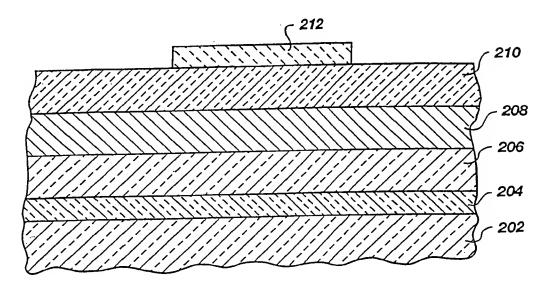


Fig. 18 (PRIOR ART)

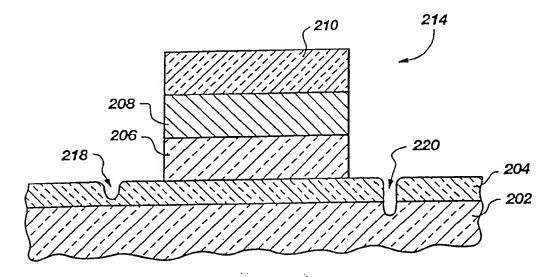


Fig. 19 (PRIOR ART)

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON

SUBSTRATE DURING GATE STACK ET Inventor: Pan et al. Serial No : 09/073 494

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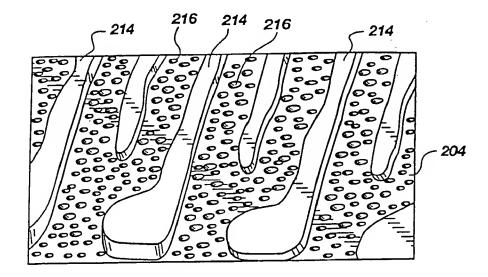


Fig. 20 (PRIOR ART)

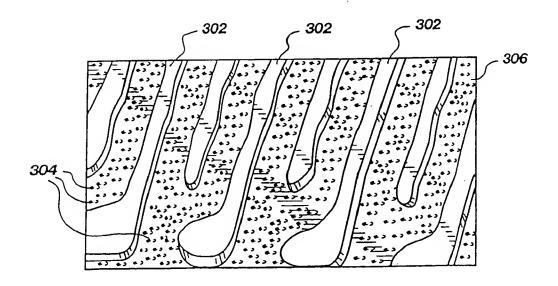


Fig. 21 (PRIOR ART)

TITLE. TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETC

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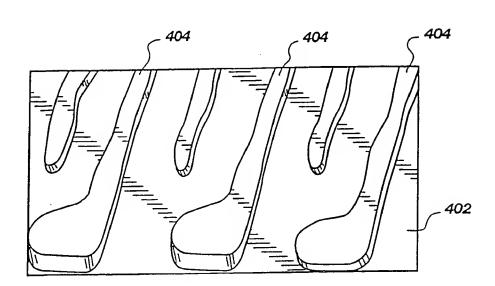


Fig. 22

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

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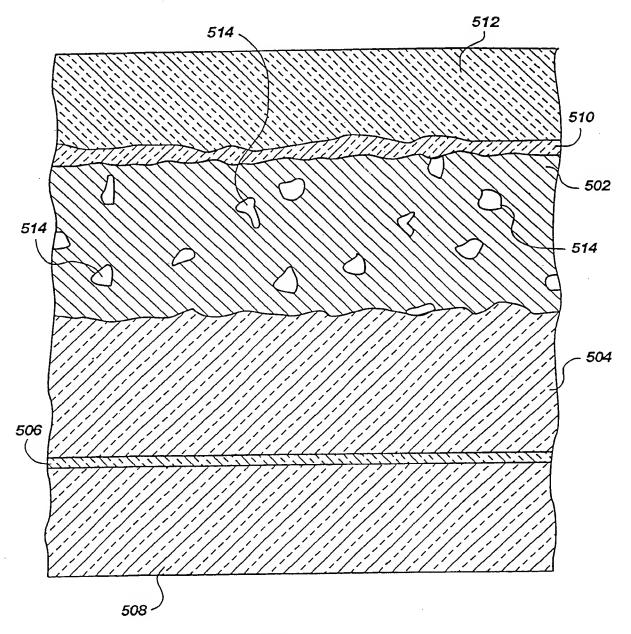


Fig. 23 (PRIOR ART)

TITLE: TECHNIQUE FOR EI IMINATION OF BITTING ON EILICONS SUBSTRATE DURING GATE STACK FECH

Inventor: Pan et al. Serial No.: 09/073,494 Docket No.: 2269-2915.1US



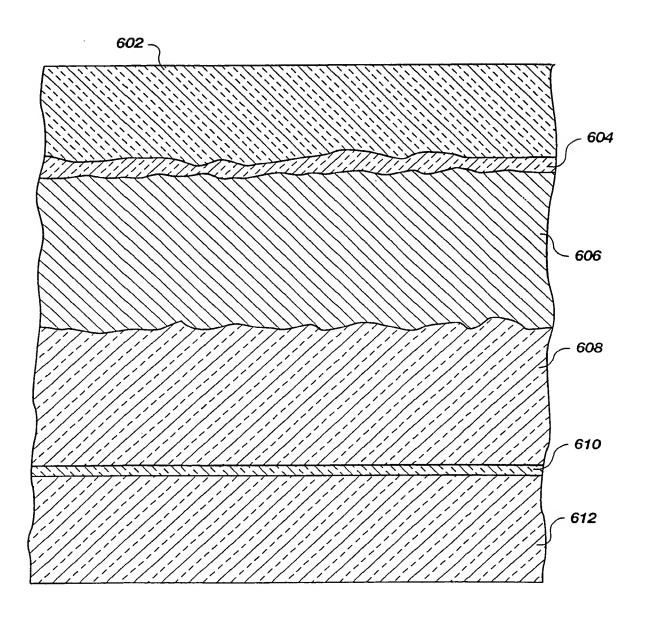


Fig. 24